Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently amended) A semiconductor device comprising:

a substrate, and

a semiconductor element area on the substrate, which includes a plurality of semiconductor elements, and a dummy area on the substrate, which includes a plurality of dummy semiconductor elements, the semiconductor element area being surrounded by the dummy area,

[[a semiconductor element on the substrate, the semiconductor element including]] wherein each of the semiconductor elements includes a first dielectric layer and an electrode on the first dielectric layer, [[and]]

[[a dummy semiconductor element on the substrate, the dummy semiconductor element including]] wherein each of the dummy semiconductor elements includes a second dielectric layer and a dummy electrode on the second dielectric layer, and

wherein each of the dummy semiconductor [[element]] elements is located so that a space between the electrode and the dummy electrode is in a predetermined range, and each of the semiconductor [[device]] elements is a transistor in which the electrode works as a gate electrode of the transistor; and said first dielectric layer is composed of [[the]] a material selected from a dielectric material having a dielectric constant of 100 or more and a ferroelectric material.

2. (Original) A semiconductor device according to claim 1, wherein the predetermined range of the space is between 0.3 μm and 14 μm.

3. (Original) A semiconductor device according to claim 1, wherein the electrode and the dummy electrode are composed of the same electrically conductive material.

4. (Original) A semiconductor device according to claim 1, wherein the first dielectric layer and the second dielectric layer are composed of the same dielectric material.

5 (Original) A semiconductor device according to claim 1, wherein the electrode is surrounded by the dummy electrode.

6. – 14. (Canceled)

15. (New) A semiconductor device comprising:

a substrate, and

a multilayer formed on the substrate, the multilayer comprising a semiconductor element and a dummy semiconductor element, and

a semiconductor element area on the substrate, which includes a plurality of the semiconductor elements, and a dummy area on the substrate, which includes a plurality of the dummy semiconductor elements, the semiconductor element area being surrounded by the dummy area,

wherein the semiconductor element includes a capacitor which is comprised of a bottom electrode, a first dielectric layer on the bottom electrode and a top electrode on the first dielectric layer, and the first dielectric layer is composed of a material selected from a dielectric material having a dielectric constant of 100 or more and a ferroelectric material,

wherein the dummy semiconductor element includes a dummy capacitor which is comprised of a dummy bottom electrode, a second dielectric layer on the dummy bottom electrode and a dummy top electrode on the second dielectric layer, and the second dielectric layer is composed of a material selected from a dielectric material having a dielectric constant of 100 or more and a ferroelectric material

wherein the dummy semiconductor element is located so that a space between the electrode and the dummy electrode is in a predetermined range, and

wherein the multilayer is produced by a method comprising:

forming a dielectric film for the first dielectric layer and the second dielectric layer;

forming an electrically conductive film on the dielectric film;

and

etching the electrically conductive film so as to form the electrode and the dummy electrode.

16. (New) A semiconductor device according to claim 15, wherein the predetermined range of the space is between 0.3μm and 14μm.

17. (New) A semiconductor device according to claim 15, wherein remnant polarization in the capacitor is in the range of 13 to 15 $\mu C/cm^2$.

18. (New) A semiconductor device according to claim 15, wherein the first dielectric layer and the second dielectric layer are composed of a material selected from $SrBi_xTa_xO_y$, $Ba_xSr_{1-x}TiO_x$, $Pb(Zr_{1-x}Ti_x)O_3$, $SrBi_2(Ta_{1-x}Nb_x)_2O_9$ or $Bi_4Ti_3O_{12}$, where $0 \leq x \leq 1$.